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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/657,068	09/09/2003	Toshiaki Iwamatsu	241807US-2DIV	9191	
22850 73	590 10/22/2004		EXAMINER		
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET			HUYNH, ANDY		
ALEXANDRIA			ART UNIT PAPER NUMBER		
			2818	···	
			DATE MAILED: 10/22/2004		

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.	Applicant(s)				
Office Action Summary		10/657,068	IWAMATSU ET AL.				
		Examiner	Art Unit				
		Andy Huynh	2818				
Period fe	The MAILING DATE of this communication app or Reply	ears on the cover sheet wit	h the correspondence addre	ss			
THE - External after - If the - If NO - Fails	ORTENED STATUTORY PERIOD FOR REPLY MAILING DATE OF THIS COMMUNICATION.  Insigns of time may be available under the provisions of 37 CFR 1.13 SIX (6) MONTHS from the mailing date of this communication.  The period for reply specified above is less than thirty (30) days, a reply of period for reply is specified above, the maximum statutory period we are to reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a re within the statutory minimum of thirty will apply and will expire SIX (6) MONT cause the application to become ABA	eply be timely filed  (30) days will be considered timely.  THS from the mailing date of this comm  ANDONED (35 U.S.C. § 133).	unication.			
Status							
1)	Responsive to communication(s) filed on 30 Se	eptember 2004.					
2a) <u></u> ☐	This action is <b>FINAL</b> . 2b) This action is non-final.						
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposit	ion of Claims						
5)□ 6)⊠ 7)□	Claim(s) <u>11-27</u> is/are pending in the application 4a) Of the above claim(s) <u>13-27</u> is/are withdraw Claim(s) is/are allowed.  Claim(s) <u>11 and 12</u> is/are rejected.  Claim(s) is/are objected to.  Claim(s) are subject to restriction and/or	vn from consideration.					
Applicat	ion Papers	•					
10)⊠	The specification is objected to by the Examine The drawing(s) filed on <u>09 September 2003</u> is/a Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct The oath or declaration is objected to by the Ex	are: a) accepted or b) are: a) accepted or b) are drawing(s) be held in abeyandion is required if the drawing(	ce. See 37 CFR 1.85(a). s) is objected to. See 37 CFR	1.121(d).			
Priority	under 35 U.S.C. § 119						
12)⊠ a)	Acknowledgment is made of a claim for foreign All b) Some * c) None of:  1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority document application from the International Bureau See the attached detailed Office action for a list	s have been received. s have been received in Aprity documents have been u (PCT Rule 17.2(a)).	pplication No. <u>09/985,020</u> . received in this National Sta	age			
2) Notice 3) Infor	et(s) ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) er No(s)/Mail Date 9903,123003;22404.	Paper No(s	ummary (PTO-413) )/Mail Date formal Patent Application (PTO-15	52)			

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#### **DETAILED ACTION**

#### Election/Restrictions

In the Response to the Election of Species Requirement dated 09/30/2004,
Applicants have elected with traverse Species A (claims 11-12 and 22-25) is
acknowledged. However, Applicants believe that claims 22-25 are not readable on
Species A. Examiner respectfully agrees with Applicants that the semiconductor of
claims 11-12 is shown in Figure 32, and the semiconductor of claims 22-25 is shown in
Figure 52. Figures 32 and 52 are two different embodiments. Thus, an election of claims
11-12 and 22-25 is further required. Applicants further elect claims 11-12 for
examination on the merits is acknowledged. Accordingly, claims 13-27 are withdrawn
from consideration as being directed to a non-elected invention. See 37 CFR 35 §
1.142(b) and MPEP § 821.03. Applicants have the right to file a divisional application
covering the subject matter of the non-elected claims 13-27.

#### **Priority**

Acknowledgment is made of applicants' claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in Parent Application No. 09/985,020, filed November 01, 2001.

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## Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 09/09/2003, 12/30/2003 and 02/24/2004. The references cited on the PTOL 1449 form have been considered.

### Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Verrett (USP: 5,612,243) in view of Korean Patent Application Laid-Open No. 1996-0002744 (English Extract), Applicant's submitted prior art (ASPA).

Verrett discloses in Fig. 1 and the corresponding texts as set forth in column 3, lines 14-30, a semiconductor device comprises:

a semiconductor layer containing a P-well (14) and a N-well (12);

a plurality of semiconductor elements (8, 9, 24 and 25) formed on said semiconductor layer;

an isolation film (16a, 16b and 16c) provided in a surface of said semiconductor layer, said semiconductor elements being electrically isolated from each other by said isolation film; and

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a PN junction portion formed by two semiconductor regions of different conductivity types (P-Si and N-Si) in said semiconductor layer provided under said isolation film.

Verrett fails to teach the isolation film including a nitride film provided in a position corresponding to a top of said PN junction portion and having a substantially uniform thickness across said two semiconductor regions; and an upper oxide film and a lower oxide film which are provided in upper and lower portions of said nitride film.

Korean Patent Application No. 1996-0002744 teaches that an element isolation film of a semiconductor element in which a trench is formed on a silicon substrate in order to increase the size of a cell region by minimizing an element isolation region and the reliability of an element can be improved by forming within the trench an element isolation film of laminated structure with good isolation property of oxide film-nitride film-oxide film.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form an element isolation film of laminated structure with good isolation property of oxide film-nitride film-oxide film, as taught by Korean Patent Application No. 1996-0002744 to incorporate into Verrett's structure to modify and to form the isolation film of Verrett's structure with an element isolation film of laminated structure with good isolation property of oxide film-nitride film-oxide film in order to improve the reliability of an device.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Verrett (USP: 5,612,243) in view of Korean Patent Application Laid-Open No. 1996-0002744

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(English Extract), Applicant's submitted prior art (ASPA), further in view of Fig. 65 of Applicants' admitted prior art (AAPA).

Verrett and Korean Patent Application No. 1996-0002744 disclose the claimed limitations except for the semiconductor device wherein said semiconductor device is an SOI semiconductor device formed on an SOI substrate including a silicon substrate, a buried oxide film provided on said silicon substrate and an SOI layer provided on said buried oxide film, said semiconductor layer being said SOI layer. However, Fig. 65 of AAPA teaches that the semiconductor device is an SOI semiconductor device formed on an SOI substrate (10) including a silicon substrate (1), a buried oxide film (2) provided on said silicon substrate and an SOI layer (3) provided on said buried oxide film, said semiconductor layer being said SOI layer. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate an SOI substrate into Verrett's structure to form the claimed invention in order to reduce parasitic capacitance and power consumption, and an operation can be performed at a high speed (see

#### Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30.AM to 5:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

Andy Huynh

10/16/04

Patent Examiner